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| EXAMINER | |
|---|---|
| LEE, CHUN KUAN | |

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| 2181 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/725,980 | DANILAK, RADOSLAV | |
| | Examiner | Art Unit | |
| | Chun-Kuan Lee | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/15/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

**RESPONSE TO ARGUMENTS**

1. Applicant's arguments filed 07/22/2008 have been fully considered but they are not persuasive. Currently claims 1-22 are pending for examination.

2. In response to applicant's arguments (on pages 8-9) with regard to the independent claim 14 rejected under 35 U.S.C. 103(a) that AAPA teaches away from the claimed limitation because the start up need to be completed before (i.e. not after) the preparation and generation of the transaction information; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because the examiner is not relying on when the preparation and generation of the transaction information, but rather is relying on the method for preparing and generating the transaction information conventionally; additionally, AAPA does not appear to be suggesting that the resulting combination with Wilcox would not function technologically; furthermore, in considering the prior art disclosure in its entirety, AAPA's teaching of excessive amount of latency would motivate one skilled in the art to combine with Wilcox, because by combining with Wilcox latency can be reduced (Wilcox, col. 2, ll. 19-23 and col. 2, ll. 51-53).

As applicant's applying the above arguments for independent claim 14 towards the independent claims 1 and 9, the examiner will also apply the above response towards the independent claims 1 and 9.

3. In response to applicant's arguments (on page 9, 3rd paragraph to page 10, 2nd paragraph) with regard to the independent claim 14 rejected under 35 U.S.C. 103(a) that the combination of references does not teach/suggest the claimed feature that upon receiving a request for a disk I/O, transferring a command causing the startup of a disk drive, because controlling a DMA burst transfer fails to teach/suggest a command for starting up a disk drive; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, as in accordance to the examiner's preceding office action, Wilcox does teaches upon receiving a request for a disk I/O (e.g. DMA request signal), transferring a command (e.g. START command) causing the startup of a disk drive (Fig. 7, ref. 202; col. 3, ll. 40-62 and col. 5, ll. 7-41), wherein subsequent to the idle state (Fig. 7, ref. 202) as the request is received, the START command is transferred causing the startup of the disk drive.

As applicant's applying the above arguments for independent claim 14 towards the independent claims 1 and 9, the examiner will also apply the above response towards the independent claims 1 and 9.

4. In response to applicant's arguments (on page10, 3rd paragraph to page 11, 2nd paragraph) with regard to the independent claim 14 rejected under 35 U.S.C. 103(a) that the combination of references does not teach/suggest the claimed feature that subsequent to transferring the command causing the start up and before the completion

of the start up, preparing the disk transaction information, because the START command is asserted at the completion of writing the DMA transfer parameters; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, and to further clarify the examiner's reliance on Wilcox's disk I/O, it is well known that the conventional start to transfer data to disk drive is after the complete burst of data to be transferred is completely and successfully received by the disk drive controller (e.g. complete preparing disk transaction information) (col. 2, ll. 10-18); where as Wilcox's novel START command starts the transferring of data to the disk drive as soon as there is sufficient data to so (e.g. without waiting for the complete burst of data to be received); therefore, Wilcox does teach/suggest subsequent to transferring the command (e.g. START command) causing the start up and before the completion of the start up, preparing the disk transaction information (e.g. preparation of the data to be transferred 204 of Fig. 7) (Fig. 7 and col. 11, l. 38 to col. 12, l. 57), as subsequent to the assertion of the START command causing the start of disk I/O and before the completion of the disk I/O, preparing the data to be transferred (e.g. disk transaction information) (Fig. 7, ref. 204).

As applicant's applying the above arguments for independent claim 14 towards the independent claims 1 and 9, the examiner will also apply the above response towards the independent claims 1 and 9.

5. In response to applicant's arguments (on page 10, 3rd paragraph to page 11, 2nd paragraph) with regard to the independent claim 14 rejected under 35 U.S.C. 103(a)

that the combination of references does not teach/suggest the claimed feature because Wilcox's controlling a DMA burst transfer and loading the trigger address differ from a command causing the start up as claimed; applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). To summarize the examiner's preceding rejection, AAPA teaches preparing a complete data for disk I/O before sending a start signal, and in view of Wilcox's teaching to forward a start signal before preparing a complete data for disk I/O, would suggest to modify AAPA such that AAPA's start signal is send before preparing the complete data for disk I/O.

6. In response to applicant's arguments (on page 11, last paragraph to page 12, 2nd paragraph) with regard to the independent claim 14 rejected under 35 U.S.C. 103(a) that the combination of references does not teach/suggest the claimed feature of a plurality of bypass register because Wilcox teaches only a memory; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, as Wilcox's memory is utilized for reducing latency associated with disk I/O (e.g. bypass register utilized for latency reduction), wherein a plurality of data for a plurality of sectors are transferred via the utilization of

the memory, therefore the memory have a plurality of registers for storing the plurality of data (col. 11, l. 38 to col. 12, l. 57).

7. In responding to all applicant's arguments, the examiner will maintain his position and the current rejection of record.

## I. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

8. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated July 15, 2008 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

## II. REJECTIONS BASED ON PRIOR ART

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Maleck (US Patent 6,681,281) and Wilcox (US Patent 6,185,634).

10. As per claims 1, 9 and 14, AAPA teaches a computer system and method comprising:

preparing disk transaction information by packaging a plurality of PRD (physical region descriptor) data structures and a plurality of CPB (command parameter block) data structures comprising the disk transaction (Specification, page 4, ll. 9-22);

transferring the disk transaction information to the disk controller (Specification, page 4, ll. 9-24); and

implementing a disk I/O (e.g. disk transaction), wherein the disk controller processes the disk transaction information to control the disk drive (Specification, page 4, ll. 9-24).

AAPA does not teach the computer system and method for implementing a bypass method for efficient disk I/O (input output), comprising:

a processor; a system memory coupled to the processor; a bridge component coupled to the processor; and the disk controller coupled to the bridge component;

upon receiving a request for a disk I/O from …;

subsequent to transferring the command causing the startup …; and

the disk controller including a plurality of bypass registers … .

Maleck teaches a computer system and method comprising:

a processor (Fig. 1, ref. 100);

a system memory (memory and cache coupled to the north bridge 110 of Fig. 1) coupled to the processor;

a bridge component (Fig. 1, ref. 110, 120) coupled to the processor; and

a disk controller coupled to the bridge component (Fig. 1, ref. 120), as data transferring to the disk controller would be transferred via the bridge component.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Maleck's computer components into AAPA's computer system because not only are these computer components well known common devices that are utilized in the computer system, the combination would also have the benefit of providing a multi-level interrupt scheme for the computer system giving priority to time critical interrupt requests and able to incorporate into existing bus architecture (Maleck col. 1, l. 44 to col. 2, l. 46) to into obtain the invention as specified in claims 1, 9 and 14.

AAPA and Maleck do not teach the computer system and method for implementing a bypass method for efficient disk I/O (input output), comprising:

upon receiving a request for a disk I/O from ...;

subsequent to transferring the command causing the startup ...; and

the disk controller including a plurality of bypass registers ... .

Wilcox teaches a system and method comprising:

upon receiving a request for a disk I/O from an application executing on the computer system, transferring a command to the disk controller, the command causing

a start up of the disk drive coupled to the disk controller (Fig. 7, ref. 202; col. 3, ll. 40-62 and col. 5, ll. 7-41);

subsequent to transferring the command causing the startup and before the completion of said start up, preparing disk transaction information (Fig. 7 and col. 11, l. 38 to col. 12, l. 57), wherein the preparation of the disk transaction information would start before the completion of the start up, because the preparation of the data to be transferred (e.g. disk transaction information) (Fig. 7, ref. 204) commence subsequent to the assertion of the START signal; and

the disk controller including a plurality of bypass registers (Fig. 1, ref. 56) for receiving the disk transaction information (col. 11, l. 38 to col. 12, l. 57).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Wilcox's disk I/O operation into AAPA's computer system and method for the benefit of reducing latency in the transferring of data to the disk drive (Wilcox, col. 2, ll. 19-23 and col. 2, ll. 51-53) to obtain the invention as specified in claims 1, 9 and 14.

11. As per claim 2, AAPA, Maleck and Wilcox teach all the limitation of claim 1 as discussed above, where AAPA further teaches the method for disk I/O in the computer system further comprising:

preparing the disk transaction information by using a processor of the computer system (AAPA, Specification, page 4, ll. 13-14); and

transferring the disk transaction information from the processor to the disk controller (AAPA, Specification, page 4, ll. 19-22).

12. As per claim 3, AAPA, Maleck and Wilcox all the limitation of claim 3 as discussed above, where AAPA and Maleck further teach the method for disk I/O in the computer system further comprising accessing a bus coupled to the disk controller to transfer the disk transaction information from the processor to the disk controller (AAPA, Specification, page 4, ll. 19-22 and Maleck, Fig. 1).

13. As per claim 4, AAPA, Maleck and Wilcox teach all the limitation of claim 3 as discussed above, where AAPA and Maleck further teach the method for disk I/O in the computer system further comprising accessing the bridge component (Maleck, Fig. 1, ref. 110, 120) controlling the bus coupled to the disk controller and transferring the disk transaction information from the processor to the disk controller via the bridge component (AAPA, Specification, page 4, ll. 19-22 and Maleck, Fig. 1).

14. As per claim 5, AAPA, Maleck and Wilcox teach all the limitation of claim 4 as discussed above, where Maleck further teaches the method for disk I/O in the computer system further comprising wherein the bridge component is a South bridge (Maleck, Fig. 1, ref. 120) of the computer system.

15. As per claim 6, AAPA, Maleck and Wilcox teach all the limitation of claim 1 as discussed above, where Wilcox further teaches the method for disk I/O in the computer system further comprising wherein the transferring of the command to the disk controller causing the start up of the disk drive is configured to hide a start up latency of the disk drive (Wilcox, col. 2, ll. 19-23 and col. 2, ll. 51-53).

16. As per claim 7, AAPA, Maleck and Wilcox teach all the limitation of claim 1 as discussed above, where AAPA further teaches the method for disk I/O in the computer system further comprising wherein the disk transaction information includes a plurality of PRD (physical region descriptor) data structures and a plurality of CPB (command parameter block) data structures for implementing the disk transaction (AAPA, Specification, page 4, ll. 15-22).

17. As per claim 8, AAPA, Maleck and Wilcox teach all the limitation of claim 1 as discussed above, where AAPA further teaches the method for disk I/O in the computer system further comprising wherein the disk drive is compatible with a version of the ATA standard (AAPA, Specification, page 3, ll. 13-14).

18. As per claim 10, AAPA, Maleck and Wilcox teach all the limitation of claim 9 as discussed above, where Maleck further teaches the computer readable media further comprising wherein the bridge component is a South bridge (Maleck, Fig. 1, ref. 120) of the computer system.

19. As per claim 11, AAPA, Maleck and Wilcox teach all the limitation of claim 10 as discussed above, where AAPA and Maleck further teach the computer readable media further comprising:

accessing a North bridge (Maleck, Fig. 1, ref. 110) to transfer the disk transaction information (AAPA, Specification, page 4, ll. 19-22); and

transferring the disk transaction information from the processor to the disk controller via the North bridge (Maleck, Fig. 1, ref. 110) and the South bridge (Maleck, Fig. 1, ref. 120) of the computer system (AAPA, Specification, page 4, ll. 19-22).

20. As per claim 12, AAPA, Maleck and Wilcox teach all the limitation of claim 9 as discussed above, where Wilcox further teaches the computer readable media further comprising wherein the transferring of the command to the disk controller causing the start up of the disk drive is configured to hide a start up latency of the disk drive (Wilcox, col. 2, ll. 19-23 and col. 2, ll. 51-53).

21. As per claim 13, AAPA, Maleck and Wilcox teach all the limitation of claim 9 as discussed above, where AAPA further teaches the computer readable media further comprising wherein the disk drive is compatible with a version of the ATA standard (AAPA, Specification, page 3, ll. 13-14; page 4, ll. 13-14).

22. As per claim 15, AAPA, Maleck and Wilcox teach all the limitation of claim 14 as discussed above, where AAPA further teaches the computer system further comprising:

preparing the disk transaction information by using a processor of the computer system (AAPA, Specification, page 4, ll. 13-14); and

transferring the disk transaction information from the processor to the disk controller (AAPA, Specification, page 4, ll. 19-22).

23. As per claim 16, AAPA, Maleck and Wilcox teach all the limitation of claim 14 as discussed above, where Maleck further teaches the computer readable media further comprising wherein the disk controller is integrated within bridge component (Maleck, Fig. 1, ref. 120), wherein it would have been obvious to integrate the disk controller into the south bridge.

24. As per claim 17, AAPA, Maleck and Wilcox teach all the limitation of claim 14 as discussed above, where Maleck further teaches the computer system further comprising wherein the bridge component is a South bridge (Maleck, Fig. 1, ref. 120) of the computer system.

25. As per claim 18, AAPA, Maleck and Wilcox teach all the limitation of claim 14 as discussed above, where Wilcox further teaches the computer system further comprising wherein the transferring of the command to the disk controller causing the start up of the

disk drive is configured to hide a start up latency of the disk drive (Wilcox, col. 2, ll. 19-23 and col. 2, ll. 51-53).

26. As per claim 19, AAPA, Maleck and Wilcox teach all the limitation of claim 14 as discussed above, where AAPA further teaches the computer system further comprising wherein the disk transaction information includes a plurality of PRD (physical region descriptor) data structures and a plurality of CPB (command parameter block) data structures for implementing the disk transaction (AAPA, Specification, page 4, ll. 15-22).

27. As per claim 20, AAPA, Maleck and Wilcox teach all the limitation of claim 14 as discussed above, where AAPA further teaches the computer system further comprising wherein the disk drive is compatible with a version of the ATA standard (AAPA, Specification, page 3, ll. 13-14; page 4, ll. 13-14).

28. As per claim 21, AAPA, Maleck and Wilcox teach all the limitation of claim 20 as discussed above, where Wilcox further teaches the computer system further comprising wherein said plurality of bypass registers is operable to allow said disk controller to implement a disk transaction without writing to a register of said ATA standard (Wilcox, col. 11, ll. 38-62).

29. As per claim 22, AAPA, Maleck and Wilcox teach all the limitation of claim 1 as discussed above, where Wilcox further teaches the method further comprising

aggregating said transaction information via a memory mapped data transfer from a processor (e.g. controller) of said computer system (Wilcox, Fig. 1, ref. 40, 42 and col. 3, l. 63 to col. 4, l. 3).

**III. CLOSING COMMENTS**

***Conclusion***

**a. STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

**a(1) CLAIMS REJECTED IN THE APPLICATION**

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

**b. DIRECTION OF FUTURE CORRESPONDENCES**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

## IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C.K.L./

September 02, 2008

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181